CLAIMS

What is claimed is:

1. An SDRAM access control unit for use with an SDRAM chip for controlling a burst transfer access operation on the SDRAM chip wherein the burst transfer access operation is preset to a specified burst data amount;

the SDRAM access control unit comprising:

an address mapping table, which is used to receive a data access request signal and related address signal for the burst transfer access operation and translate the received address signal into corresponding addresses in the SDRAM chip;

an access control logic circuit, which is used to control the burst transfer access operation based on specified mode and burst data length;

a configuration register, which is used to register the configuration parameters of the clocking of various signals of the SDRAM chip;

a column address control module, which is used for control of row addresses during the burst transfer access operation; and

a finite state machine, which is capable of generating a set of access control signals based on data from the address mapping table, the access control logic circuit, and the column address control module for control of the burst transfer access operation to the SDRAM chip;

wherein

each burst transfer access operation is performed in such a manner that:

during a first clock pulse, a column address strobe signal and a column address signal are issued to the SDRAM chip;

during a second clock pulse, the column address strobe signal is disabled; and

during subsequent clock pulses, a column address strobe signal is continuously maintained at enabled state while a sequence of column address signals are successively issued to the SDRAM chip for retrieval of the requested data in the burst transfer access operation.

2. The SDRAM access control unit of claim 1, wherein the SDRAM chip is a DDR SDRAM chip.

3. The SDRAM access control unit of claim 1, wherein in the case of the burst transfer access operation being a write operation, the data are written into the SDRAM chip in synchronization with the column address strobe signal.

4. The SDRAM access control unit of claim 1, wherein in the case of the burst transfer access operation being a read operation, the retrieved data from the SDRAM chip are delayed by a latency period with respect to the column address strobe signal.

5. An SDRAM access control method for use on an SDRAM chip for controlling a burst transfer access operation on the SDRAM chip wherein the burst transfer access operation is preset to a specified burst data amount;

the SDRAM access control method comprising:

during a first clock pulse, issuing a column address strobe signal and a column address signal to the SDRAM chip;

during a second clock pulse, disabling the column address strobe signal; and

during subsequent clock pulses, continuously maintaining a column address strobe signal at enabled state while a sequence of column address signals are successively issued to the SDRAM chip for retrieval of the requested data in the burst transfer access operation.

6. The SDRAM access control method of claim 5, wherein the SDRAM chip is a DDR SDRAM chip.

7. The SDRAM access control method of claim 4, wherein in the case of the burst transfer access operation being a write operation, the data are written into the SDRAM chip in synchronization with the column address strobe signal.

8. The SDRAM access control method of claim 4, wherein in the case of the burst transfer access operation being a read operation, the retrieved data from the SDRAM chip are delayed by a latency period with respect to the column address strobe signal.

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